**MADHU SHREE M B** 

Electronics and Comminications Engineering

Dayananda Sagar College of Engineeering

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**Career Objective**

To pursue a challenging career with dedication and provide my efficiency to the fullest in a professional organization environment wherever I serve my duties that will discover the potential .

**Academic Qualifications**

| **Qualification** | **University / Board** | **Institution** | **Year of**  **Passing** | **Percentage** |
| --- | --- | --- | --- | --- |
| BE (E & C) | Visvesvaraya Technological University) | Dayananda Sagar  College of Engineering | 2023  (Pursuing) | 8.76(aggr.) |
| 12th | Department of Pre University Education (Karnataka) | Alvas PU college | 2019 | 94.33 |
| 10th | KSEEB (Karnataka) | Sri Venu Vidya Samasthe | 2017 | 98.40 |

***\*8th Semester***

**Technical Skills**

**Programming Languages**: C ,Python,Verilog, System Verilog,UVM

**Operating System**: Linux

**Scripting Languages**: perl scripting

**Core Skills**: RTL Coding using Synthesizable constructs of Verilog, FSM

based design, Simulation, CMOS Fundamentals

**Static timing Analysis:** Types,False path,SYA in design flow,clock,timing parameters.

**Digital Electronics**: Combinational & Sequential circuits, FSM, Memories, CMOS – fabrication and implementation, Stick diagram

**Simulation tools:** Matlab ,quatus prime, Modelsim, virtual box, Ubantu, cadence,Multisim,NS2

**Workshops / Seminars / Trainings Attended**

✓ **CANSAT** – A workshop is done related to a can sized satellite that gave information about humidity and pressure which was developed using Arduino board and different sensors 2020 February

✓ **VLSI DESIGN AND VERIFICATION**

I'm undergoing a training for VLSI design and verification at Maven Silicon Banglore in online mode

Mar 2022 – Present (Ongoing)

**INTERNSHIP**

Has successfully completed internship program on embedded systems from psi borg technologies in associated with teachnook

From 1st of august 2022 to 30 of september 2022

**PROJECT**

**Controlled Area Network (CAN) Using Verilog**

* HDL:Verilog
* EDA Tools:Modelsim
* Description: CAN protocol is a standard designed to allow the microcontroller and other devices to communicate with each other without any host computer.

**Router 1x3 – RTL design** ( July 2022 – August 2022)

* HDL: Verilog
* EDA Tools: Modelsim, Quartus-prime
* Description: The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1 and channel2.

**Implementation of palm vein image processing and enhancement on FPGA** (ongoing)

* HDL:Verilog
* Tools :Modelsim,Quartus-prime,Matlab
* Description: to develop a low cost but efficient system for image processing and enhancement of the acquired image of the palm vein obtained by the infrared rays.

**INTERPERSONAL SKILLS**

Hard Work, Detemination, Empathy, Adaptabiliy, Negotiation, creativity, leadership

**PERSONAL DETAILS**

Date of Birth: 26th february 2002

Mothers’ Name: Sudha H V

Fathers’ Name: Byrareddy M S

Language Known:, Kannada, English,Telugu,Hindi

Permanent Address:Maniganahalli(v), Srinivaspura (T),kolar(D),Karnataka-563135

hobbies :Drawing, watching K drama, music

*I hereby declare that the information given by me is true to the best of my knowledge.*

Place: Bangalore **MADHU SHREE M B**